Amendments to the Claims:

This listing of claims will replace all prior versions and listings of claims in the application.

Listing of Claims:

Claim 1. (Currently Amended) A method of developing an ASIC comprising:

developing a hardware model including a CPU bus functional model, and a software ~~coupled to~~ **loaded on** a CPU server concurrently;

communicating command and control information between the CPU server and the CPU bus functional model over a network according to an XBUS protocol **modified to exchange data for all modules using the XBUS protocol by sharing a plurality of registers and without using a physical bus**;

co-simulating the hardware model and the software; and

receiving real working environment test inputs for the co-simulation.

Claim 2. (Previously Presented) The method of claim 1, wherein the hardware model is developed on a workstation.

Claim 3. (Original) The method of claim 1, wherein the software is developed on a target board.

Claim 4. (Canceled)

Claim 5. (Previously Presented) The method of claim 1, wherein the co-simulated hardware model is described by a high-level language model.

Claim 6. (Canceled)

Claim 7. (Canceled)

Claim 8. (Currently Amended) A method of co-simulating a hardware model and a software in ASIC development, comprising:

Requesting, by a hardware side including a **hardware model and a** CPU bus functional model, access to a software side[[,]] including a **software loaded on** CPU server[[,]] over a network according to ~~an~~ **a modified** XBUS protocol **to exchange data for all modules using the XBUS protocol by sharing a plurality of registers and without using a physical bus**;

invoking a function call by the CPU server;

sending an access request from the CPU bus functional model to the CPU server over the network **according to the modified XBUS protocol**;

routing the access request to the hardware model;

co-simulating the hardware model and the software; and

receiving real working environment test inputs for the co-simulation.

Claim 9. (Original) the method of claim 8, wherein the function call is a READ function call.

Claim 10. (Original) The method of claim 8, wherein the function call is a WRITE function call.

Claim 11. (Previously Presented) The method of claim 8, further comprising:

requesting a hardware model interrupt; and

handling the hardware model interrupt with a function call invoked by the ~~software component~~ **CPU server** over the network.

Claim 12. (Currently Amended) An apparatus for hardware model and software co-simulation in ASIC development, comprising:

a hardware model including a CPU bus functional model to represent a hardware board circuit;

a software ~~coupled to~~ **to load on** a CPU server to provide command and control access of the hardware model;

a network coupled to the CPU bus functional model and the CPU server to communicate a command from the software to the hardware model and to route contents of the command between the hardware model and software according to ~~an~~ **a modified** XBUS protocol **to exchange data without using a physical bus** to provide co-simulation of the hardware model and software**; and**

a plurality of shared registers coupled to the hardware model and the software, the shared registers configured to communicate according to the modified XBUS protocol

wherein the hardware model is configured to receive real working environment test inputs for the co-simulation.

Claims 13-23. (Canceled)